1. (currently amended) A circuit to improve the stability of a low drop-out (LDO) voltage regulator comprising:

a means of an adaptive biased driving stage of said LDO;

an impedance, keeping the gate pole of a pass transistor close to the resonance frequency, being connected on one side to said means of an adaptive biased driving stage and on the other side to the gate of a pass device of said LDO;

said pass device of said LDO, wherein its gate is connected to said impedance and the source and drain are connected to V_{DD} voltage and to the output voltage of said LDO; and

a filter capacitor being connected to ground and to the output voltage of said LDO.

2. (original) The circuit of claim **1** wherein said impedance is a resistor.

3. (original) The circuit of claim **1** wherein said impedance is provided by a transistor.

4. (original) The circuit of claim **1** wherein said impedance can be reduced during specific load conditions using an additional parallel impedance.

5. (original) The circuit of claim **4** wherein said specific load condition is a medium load condition.

6. (original) The circuit of claim **4** wherein said parallel impedance is a transistor.

7. (original) The circuit of claim **4** wherein said parallel impedance is a transistor having a serial resistor.

8. (original) The circuit of claim **4** wherein said reduction of said impedance is performed in more than one step depending on the size of the load current.

9. (original) The circuit of claim **8** wherein said reduction of impedance is performed by adding in each step an additional parallel impedance to the first impedance.

10. (original) The circuit of claim **9** wherein said additional parallel impedances are formed by parallel arranged transistors.

11. (original) The circuit of claim **8** wherein said additional parallel impedances are formed by parallel arranged transistors having a serial resistor.

12. (original) The circuit of claim **4** wherein a special circuitry detects said specific load conditions and initiates said reduction of the impedance connected to the gate of said pass device depending on the size of the load current of said LDO.

13. (original) The circuit of claim **12** wherein said specific load condition is a medium load current.

14. (original) The circuit of claim **12**, detecting a specific load condition and initiating a reduction of the gate impedance of said pass device in one step, wherein said

special circuitry comprises a current source connected to ground and to a first transistor, which is connected via two additional transistors, acting as level shifters to V_{DD} voltage and furthermore the gate of said first transistor is connected to said current source and to the gate of a second transistor, which is connected to ground and to a third transistor, which is connected to VDD, and to the gate of said transistor, being a shunt to the impedance to be reduced, and wherein the gate of said third transistor is connected to the impedance to be reduced.

15. (original) The circuit of claim **12**, detecting a specific load condition and initiating a reduction of the gate impedance of said pass device in more than one step, wherein said special circuitry comprises a current source connected to ground and to a first transistor, which is connected via two additional transistors, acting as level shifters to V_{DD} voltage and furthermore the gate of said first transistor is connected to said current source and to the gate of a second transistor, which is connected to ground and to a third transistor, which is connected to VDD, and to the gate of said transistor, being a shunt to the impedance to be reduced, and wherein the gate of said third transistor is connected to the impedance to be reduced, and wherein for each additional step of impedance reduction two additional transistors in parallel to said second and third transistors are introduced, which are controlling the gate of one for each step additional transistor which is an additional shunt to the impedance to be reduced.

16. (currently amended) A method to improve the stability of a low drop-out (LDO) voltage regulator comprising:

providing a pass device for an adaptive biased driving stage;

add a serial impedance to the gate capacitance of said pass device in order to keep the gate pole of said pass device close to the resonance frequency; and

shunt partly said impedance in case of medium load currents as far as required.

17. (original) The method of claim **16** wherein said adaptive biased driving stage is a gm-buffer.

18. (original) The method of claim **16** wherein said adaptive biased driving stage is a current mirror.

19. (original) The method of claim **14** wherein said serial impedance is a transistor.

20. (original) The method of claim **14** wherein said serial impedance is a resistor.

21. (original) The method of claim **14** wherein said serial impedance is shunted by a transistor.

22. (original) The method of claim **14** wherein said serial impedance is shunted by a transistor having a serial resistor.

23. (original) The method of claim **14** wherein said serial impedance is shunted in more than one step.